AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of the claims in the application.

Listing of Claims

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Currently Amended) A thin film transistor ("TFT") array panel comprising:

first and second gate lines transmitting gate signals to adjacent pixel ~~rows~~ electrodes and disposed adjacent to each other;

a data line insulated from the first and the second gate lines ~~and the data line~~;

a first thin film transistor connected to the first gate line and the data line, and including a first drain electrode overlapping the second gate line;

a second thin film transistor ~~TFT~~ connected to the second gate line and the data line, disposed opposite the first thin film transistor ~~TFT~~ with respect to the data line, and including a second drain electrode overlapping the first gate line;

a first pixel electrode connected to the first drain electrode and overlapping the second gate line; and

a second pixel electrode connected to the second drain electrode and overlapping the first gate line.

8. (Original) The TFT array panel of claim 1, further comprising red, green or blue color filters disposed in a pixel area defined by intersections of the first and the second gate lines and the data line.

9. (Original) The TFT array panel of claim 1, wherein the first and the second TFTs comprise:

first and second gate electrodes connected to the first and the second gate lines, respectively;

first and second semiconductors overlapping the first and the second gate electrodes, respectively; and

first and second source electrodes connected to the data line and overlapping the first and the second semiconductors, respectively.

10. (Original) The TFT array panel of claim 2, wherein the first and the second TFTs comprise:

first and second gate electrodes connected to the first and the second gate lines, respectively;

first and second semiconductors overlapping the first and the second gate electrodes, respectively; and

first and second source electrodes connected to the data line and overlapping the first and the second semiconductors, respectively.

11. (Original) The TFT array panel of claim 4, further comprising a passivation layer interposed between the first and the second TFTs and the first and the second pixel electrodes and including organic insulator or inorganic insulator.

12. (Currently Amended) The TFT array panel of claim 5, wherein the passivation layer includes a first and a second contact holes ~~to respectively connect~~ exposing the first and the second drain electrodes, and the first and the second pixel electrodes are connected to the first and the second drain electrodes through the contact holes.

13. (Currently Amended) The TFT array panel of claim 6, wherein the first contact hole overlaps the second gate line and the second contact hole overlaps the first gate line.

14. (Original) The TFT array panel of claim 1, wherein the first pixel electrode does not overlap the first gate line, and the second pixel electrode does not overlap the second gate line.

15. (Original) The TFT array panel of claim 1, wherein the first and the second pixel electrodes overlap the data line.